



PJMG20N40DL

N-Channel Enhancement Mode Power MOSFET

Product Summary

- $V_{DS} = 40V, I_D = 26A$
- $R_{DS(on)} < 14m\Omega @ V_{GS} = 10V$
- $R_{DS(on)} < 19.5m\Omega @ V_{GS} = 4.5V$

Features

- Advanced Split Gate Trench Technology
- 100% Avalanche Tested
- 100% DVDS
- RoHS and Reach Compliant
- Halogen and Antimony Free
- Moisture Sensitivity Level 3
- Molding Compound Meets UL 94 V-0 Flammability Rating

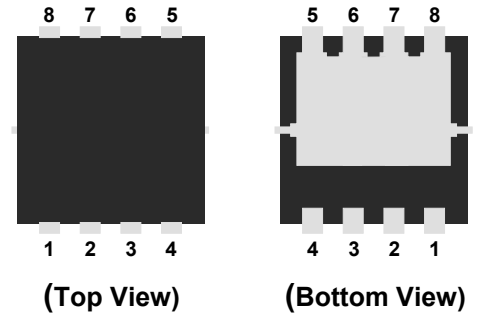
Application

- Load Switch
- PWM Application
- Power Management

Marking Code

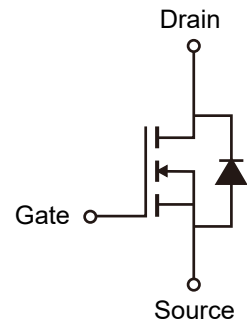


PDFN3x3-8L



Pin	Description
1,2,3	Source
4	Gate
5,6,7,8	Drain

Schematic Diagram



Absolute Maximum Ratings

Ratings at 25°C case temperature unless otherwise specified.

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous	$T_C = 25^\circ C$	I_D	26	A
	$T_C = 100^\circ C$		16	
Drain Current-Pulsed ^{Note1}		I_{DM}	104	A
Single Pulse Avalanche Energy ^{Note2}		E_{AS}	16	mJ
Maximum Power Dissipation		P_D	20	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Characteristics

Thermal Resistance, Junction-to-Ambient ^{Note3}	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.3	°C/W



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Electrical Characteristics

(T_J=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	40	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage ^{Note4}	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2.5	V
Drain-Source On-Resistance ^{Note4}	R _{DS(on)}	V _{GS} =10V, I _D =10A	--	11	14	mΩ
		V _{GS} =4.5V, I _D =5A	--	15	19.5	mΩ
Forward Transconductance ^{Note4}	g _{FS}	V _{DS} =5V, I _D =5A	--	8.5	--	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHz	--	396	--	pF
Output Capacitance	C _{oss}		--	119	--	pF
Reverse Transfer Capacitance	C _{rss}		--	13	--	pF
Gate resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz	--	2.2	--	Ω
Total Gate Charge	Q _g	V _{DS} =20V, I _D =5A, V _{GS} =10V	--	7	--	nC
Gate-Source Charge	Q _{gs}		--	2	--	nC
Gate-Drain Charge	Q _{gd}		--	1.5	--	nC
Switching Characteristics						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, I _D =5A, V _{GS} =10V, R _{GEN} =6Ω	--	12	--	nS
Turn-on Rise Time	t _r		--	14	--	nS
Turn-off Delay Time	t _{d(off)}		--	24	--	nS
Turn-off Fall Time	t _f		--	20	--	nS
Source-Drain Diode Characteristics						
Diode Forward Voltage ^{Note4}	V _{SD}	V _{GS} =0V, I _S =5A	--	--	1.2	V
Diode Forward Current	I _S		--	--	26	A
Reverse Recovery Time	t _{rr}	I _F =5A, di/dt=100A/μS	--	18	--	nS
Reverse Recovery Charge	Q _{rr}		--	13	--	nC

Note:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. E_{AS} condition: T_J=25°C, V_{DD}=20V, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=8A
3. Surface mounted on 1inch² FR-4 board with 2OZ copper
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Test Circuit

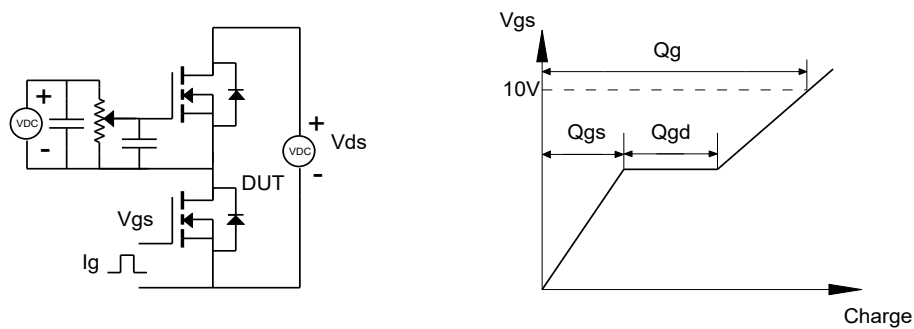


Figure 1: Gate Charge Test Circuit & Waveform

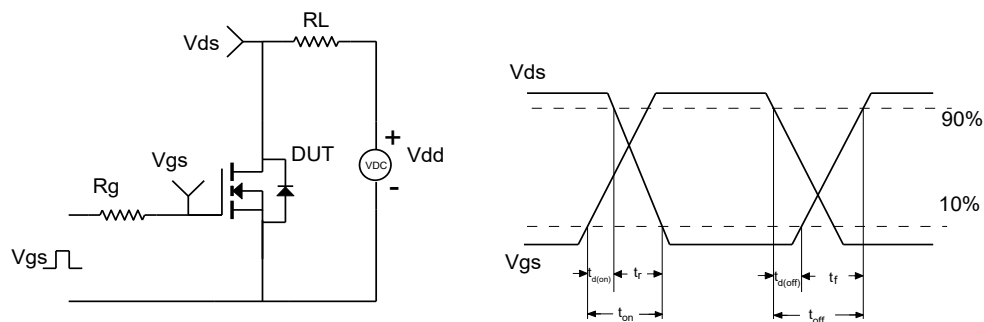


Figure 2: Resistive Switching Test Circuit & Waveform

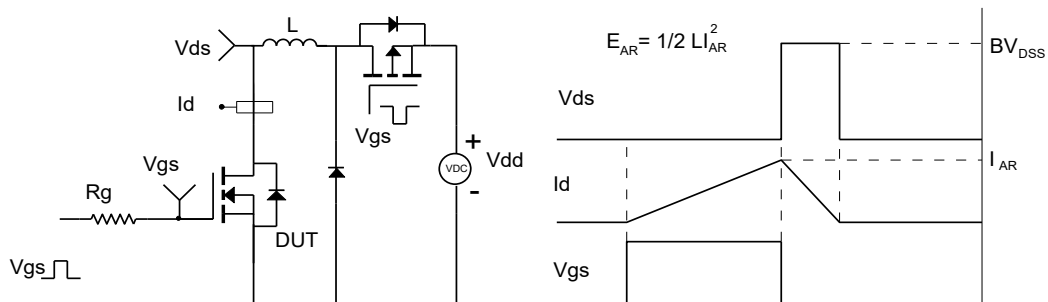


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

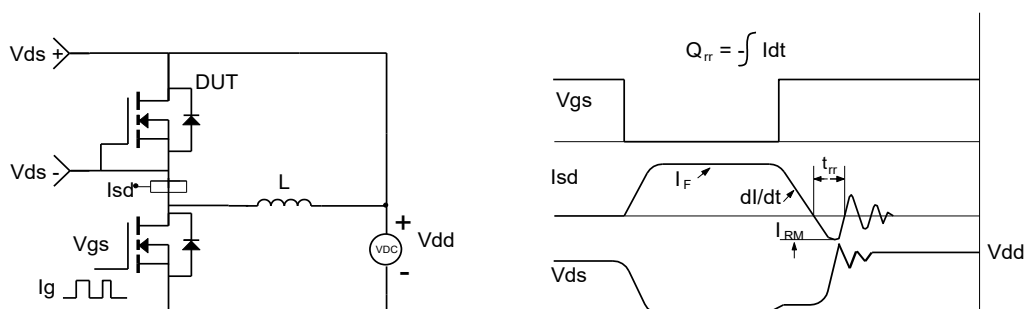


Figure 4: Diode Recovery Test Circuit & Waveform

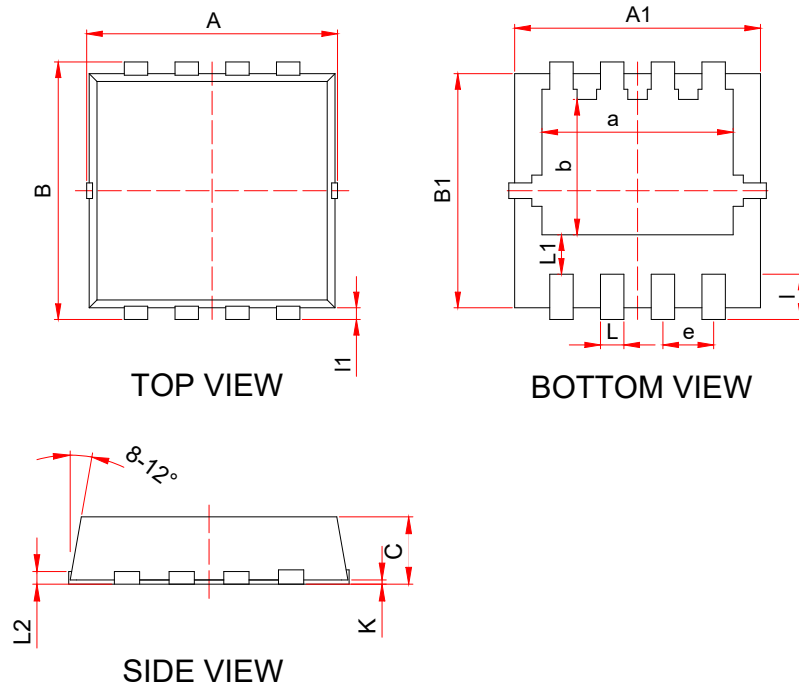


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Package Outline

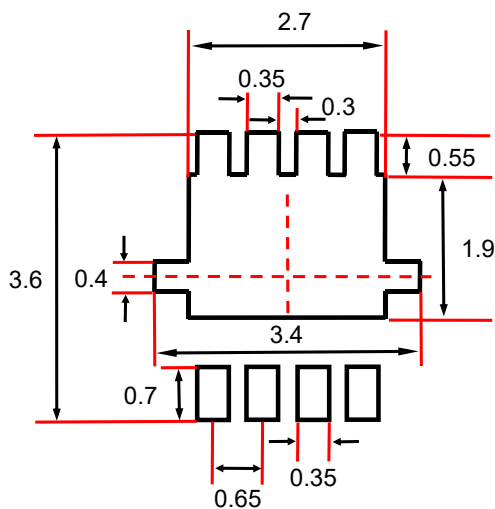
PDFN3x3-8L



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	3.100	3.200	3.300	0.122	0.126	0.130
A1	3.050	3.150	3.250	0.120	0.124	0.128
a	2.350	2.450	2.550	0.093	0.096	0.100
B	3.200	3.300	3.400	0.126	0.130	0.134
B1	2.900	3.000	3.100	0.114	0.118	0.122
b	1.650	1.750	1.850	0.065	0.069	0.073
C	0.750	0.800	0.850	0.030	0.031	0.033
L	0.250	0.300	0.350	0.010	0.012	0.014
L1	0.600	0.700	0.800	0.024	0.028	0.031
L2	0.140	0.160	0.180	0.005	0.006	0.007
I	0.300	0.400	0.500	0.012	0.016	0.020
I1	0.120	0.150	0.180	0.005	0.006	0.007
K	0.000	-	0.050	0.000	-	0.002
e	0.550	0.650	0.750	0.022	0.026	0.030

Suggested Pad Layout

PDFN3x3-8L



Note:

1. Package Body Sizes Exclude Mold Flash and Gate Burrs
2. Controlling Dimension: In millimeters
3. General Tolerance: $\pm 0.05\text{mm}$
4. The Pad Layout is for reference purposes only

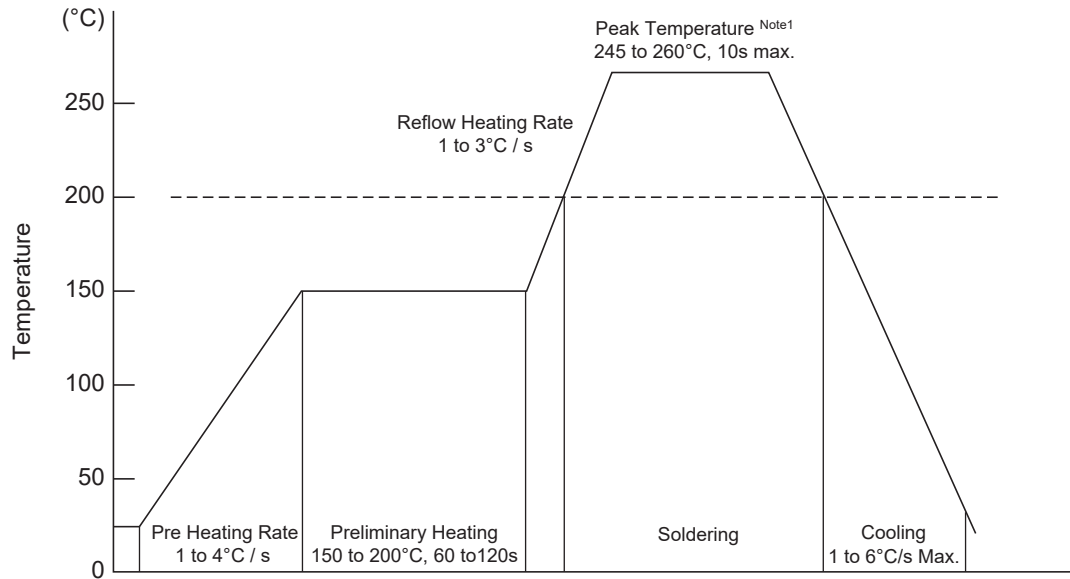


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Conditions of Soldering and Storage

◆ Recommended condition of Reflow Soldering(Pb-Free Solder)



Recommended peak temperature is over 245°C. If peak temperature is below 245°C, you may adjust the following parameters:

- Time length of peak temperature (longer)
- Time length of soldering (longer)
- Thickness of solder paste (thicker)

Note1:

Maximum thermal excursion allowed during the reflow assembly is as follow:

- Temperature: 255°C~260°C
- Duration at peak soak : 30 seconds
- Number of reflow: 3
- **Conditions of hand soldering** ^{Note2}

- Temperature: 320±10°C
- Time: 3s max.
- Times: one time

Note2: Not recommended for mass production, an engineering project, or re-work, it is allowed. It should be used with caution

● **Storage conditions**

● **Temperature**

5 to 30°C

● **Humidity**

≤ 60% RH

● **Floor Life**

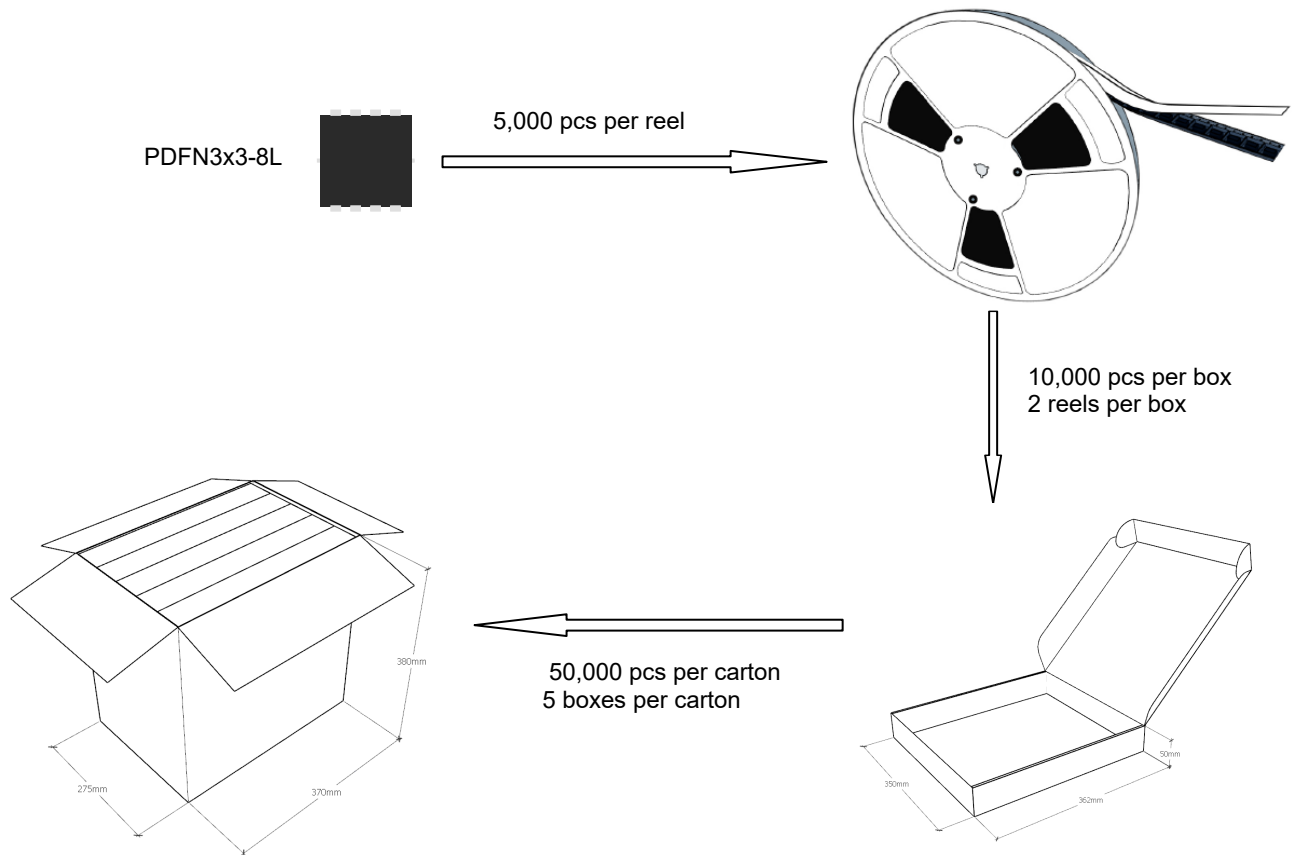
168 Hours

● **Recommended period**

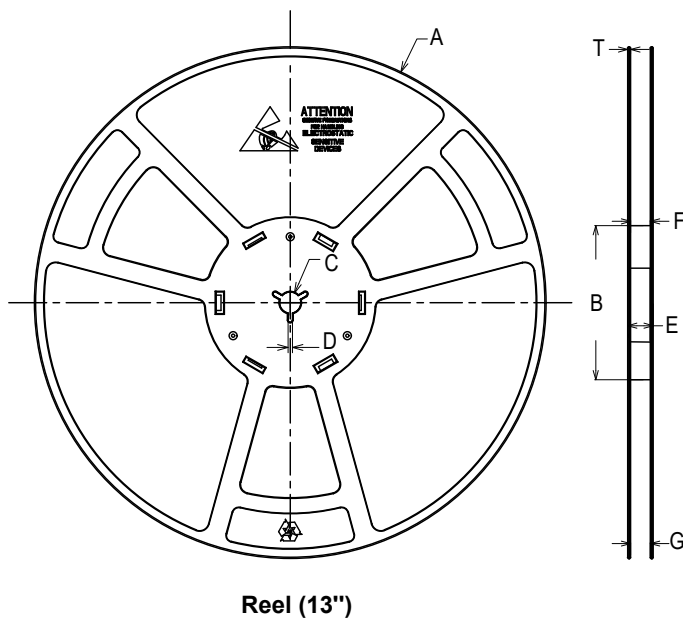
Five year after manufacturing(Depends on storage conditions)

Package Specifications

- The method of packaging



reel data



Symbol	Value(unit:mm)
A	$\Phi 330 \pm 2$
B	$\Phi 99.5 \pm 0.5$
C	13.6 ± 0.3
D	2.8 ± 0.2
E	16.2 ± 0.5
F	$13^{+0.8}_{-0.3}$
G	13 ± 3
T	1.6 ± 0.2



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◆ Embossed tape data

